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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/687,460	10/15/2003	Tetsuo Hironaka	SUSU121842	8870

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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/687,460	HIRONAKA ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *5-15 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/15/03&2/6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

1. Examiner noticed that there was a typo error for the Group I claims in the Election/restrictions filed on 07/03/2006, Applicant's election without traverse of claims 5-15 and 17 are cancelled, and claims 1-4 and 16 are pending in the application in the reply filed on 08/21/2006 is acknowledged. Thus, this Office action is in response to claims 1-4 and 16.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

3. The drawings filed on 10/15/2003 have been approved by the Examiner.

Oath/Declaration

4. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

Information Disclosure Statement

5. The information disclosure statement (IDS) submitted on 10/15/2003 and 02/06/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

6. Claim 3 is objected to because of the following informalities:

in claim 3, last line, "HMA" should be changed to –hierarchical multi-port memory architecture--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et al., US 5,784,630

Regarding claim 1, Saito (first embodiment) teaches a multi-port instruction/data integrated cache (it is taught as the cache memory A5, col.7, lines 59-61) which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle (col.8, lines 9-12) and a main memory (main memory A4) and which stores a part of instructions and data stored in the main memory (Fig.1 and col.7, lines 57-59), comprising:

a plurality of ports (col.10, lines 22-24) including an instruction port unit consisting of at least one instruction port used to access an instruction from the parallel processor (Fig.5, col.15, lines 50-52), and a data port unit consisting of at

least one data port used to access data from the parallel processor (Fig.5, col.15, lines 52-53), wherein a data width which can be specified to the bank from the instruction port is set larger than a data width which can be specified to the bank from the data port (col.15, lines 38-44 and lines 56-59).

The first embodiment of Saito does not clearly teach a cache memory having a plurality of banks;

However, the secondary embodiment of Saito teaches a cache memory is divided into a plurality of cache banks (col.6, lines 16-18 and col.31, line 1-17 and col.32, lines 59-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of the second embodiment of Saito into the first embodiment of Saito such as a cache memory having a plurality of banks because the individual processors can simultaneously access the cache banks independent of one another, thus, even when a large amount of data is shared by the individual processor elements, the cache hit ratio can be increased to thereby allow the individual processor elements to execute respective processing in parallel (col.6, lines 21-27).

Regarding claim 2, Saito teaches a plurality of non-continuous banks can be accessed from the instruction port, and all the banks can be accessed from the data port (col.4, lines 54 to col.5, lines 18).

Regarding claim 3, Saito teaches the multi-port instruction/data integrated cache is constituted by an HMA structure (Fig.26).

Regarding claim 4, Saito teaches the multi-port instruction/data integrated cache is constituted by a crossbar switch network structure (Fig.26).

Regarding claim 16, Saito (first embodiment) teaches a multi-port instruction/data integrated cache (it is taught as the cache memory A5, col.7, lines 59-61) which is provided between a parallel processor to execute a plurality of types of processing in one clock cycle (col.8, lines 9-12) and a main memory (main memory A4) and which stores a part of instructions, traces and data stored in the main memory (Fig.1 and col.7, lines 57-59), comprising:

a plurality of ports (col.10, lines 22-24) including an instruction port unit consisting of at least one instruction port used to access an instruction from the parallel processor(Fig.5, col.15, lines 50-52), a trace port unit consisting of at least one trace port used to access a trace from the parallel processor (it is taught as test-and –set instruction; col.16, lines 41-52), and a data port unit consisting of at least one data port used to access data from the parallel processor(Fig.5, col.15, lines 52-53), wherein each data width which can be specified to the bank from the instruction port and the trace port is set larger than a data width which can be specified to the bank from the data port(col.15, lines 38-44 and lines 56-59).

The first embodiment of Saito does not clearly teach a cache memory having a plurality of banks;

However, the secondary embodiment of Saito teaches a cache memory is divided into a plurality of cache banks (col.6, lines 16-18 and col.31, line 1-17 and col.32, lines 59-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the teachings of the second embodiment of Saito into the first embodiment of Saito such as a cache memory having a plurality of banks because the individual processors can simultaneously access the cache banks independent of one another, thus, even when a large amount of data is shared by the individual processor elements, the cache hit ratio can be increased to thereby allow the individual processor elements to execute respective processing in parallel (col.6, lines 21-27).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsuruta et al	US 6378050 B1
Au et al	US 6754777 B1
Shibayama	US 6678789 B2
Kametani et al	US 6647465 B2
Mattausch et al	US 6845429 B2

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 7:30-5:30 (first Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jasmine Song

Patent Examiner

October 24, 2006